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TITLE: Processing system with microcomputers each operable in master and slave modes using configurable bus access control terminals and bus use priority signals

Abstract Text (1):
A single-chip microcomputer comprising: a first bus having a central processing unit and a cache memory connected therewith; a second bus having a dynamic memory access control circuit and an external bus interface connected therewith; a break controller for connecting the first bus and the second bus selectively; a third bus having a peripheral module connected therewith and having a lower-speed bus cycle than the bus cycles of the first and second buses; and a bus state controller for effecting a data transfer and a synchronization between the second bus and the third bus. The single-chip microcomputer has the three divided internal buses to reduce the load capacity upon the signal transmission paths so that the signal transmission can be accomplished at a high speed. Moreover, the peripheral module required to have no operation speed is isolated so that the power dissipation can be reduced.

Brief Summary Text (13):
A representative of the invention to be disclosed herein will be briefly described in the following. Specifically, an internal bus is divided into three: the first bus is connected with a central processing unit and a cache memory, and the second bus is connected with a dynamic memory access controller and an external bus interface. The first bus and the second bus are equipped with a break controller having a bus transceiver function to connect the first address bus and the second address bus selectively. The third bus given a lower speed than the first and second bus cycles is connected with peripheral modules. There is provided a bus state controller for data transfers and synchronizations between the second bus and the third bus.

Brief Summary Text (18):
According to the above-specified means, the peripheral modules to be connected with the third bus are the free running timer, the serial communication interface and/or the watch-dog timer, which have no direct participation in the speed-up of the data processing, so that they can be given low-speed bus cycles. Thus, the existing peripheral modules can be used as they are without following the high speed of the central processing unit, to make the design efficient and to reduce the power dissipation in the peripheral modules.

Brief Summary Text (23):
A further representative of the invention to be disclosed herein will be briefly described in the following. Specifically, the aforementioned external bus interface is given the burst read mode and the single-write mode of the synchronous dynamic type RAM, and the interface function to access the dynamic type RAM and a pseudo-static type RAM directly.

Brief Summary Text (24):
According to the above-specified means, the synchronous dynamic type RAM, the dynamic RAM and the pseudo-static type RAM can be directly connected by the external bus interface, to improve the user-friendliness.

Brief Summary Text (25):
A further representative of the invention to be disclosed herein will be briefly described in the following. Specifically, the external bus interface produces a clock pulse, which has its phase advanced from the clock pulse of the central processing unit, and feeds it to the clock terminal of the synchronous dynamic type RAM.

Brief Summary Text (29):
A further representative of the invention to be disclosed herein will be briefly described in the following. Specifically, the external bus interface is equipped with a memory control signal generator for generating a control signal necessary for setting the operation mode of the synchronous dynamic type RAM by using an address signal partially, when the central processing unit is started by accessing a predetermined access space to set a row address strobe signal (i.e., RAS), a column address strobe signal (i.e., CAS) and a write enable signal (i.e., WE) to the low level.

Drawing Description Text (9):
FIG. 8 is a block diagram showing an example of connection between the bus state controller BSC to be packaged in the single-chip microcomputer according to the present invention and a synchronous dynamic type RAM through an external bus interface OBIF;

Drawing Description Text (13):
FIG. 12 is a block diagram showing an example of connection between the bus state controller BSC to be packaged in the single-chip microcomputer according to the present invention and a dynamic type RAM through the external bus interface OBIF;

Drawing Description Text (15):
FIG. 14 is a block diagram showing an example of connection between the bus state controller BSC to be packaged in the single-chip microcomputer according to the present invention and a pseudo-static type RAM through the external bus interface OBIF;

Drawing Description Text (17):
FIG. 16 is a timing chart for explaining the case in which the SDRAM on a main bus is to be accessed from the S-MCU of FIG. 15;

Drawing Description Text (35):
FIG. 33 is a timing chart for explaining the individual bus cycles in the single-chip microcomputer according to the present invention;

Detailed Description Text (9):
Since, in this embodiment, the central processing unit CPU is connected with the first internal bus (AB1 and DB1) connected with only the cache memories (TAG, CAC, CDM) and the multiplier unit MULT, the load capacity of the bus can be drastically reduced to simplify the bus drive circuit of the central processing unit CPU for the aforementioned high-speed operations and to reduce the power dissipation of the bus drive circuit.

Detailed Description Text (10):
The second internal bus is composed of an address bus AB2 and a data bus DB2 and connected with the divider unit DIVU, the dynamic memory access controller DMAC and an external bus interface OBIF. When an access to the aforementioned cache memory is a miss hit, the central processing unit CPU has to fetch data by accessing to an external memory. For this, there is required a function to transmit an address signal on the first internal bus to the second internal bus. On the other hand, when the first and second internal buses are separated, as described above, the dynamic memory access controller DMAC may be caused by a program miss to garble the content of the data memory CDM of the cache memory.

Detailed Description Text (14):
With this, however, the data transfer with the central processing unit CPU or the like cannot be effected as it is, because the central processing unit CPU and the individual peripheral modules have different operation frequencies. Thus, there is provided a bus state controller BSC. This bus state controller BSC transmits a signal (e.g., a data signal) as it is when it transfers the signal from the third internal bus to the second internal bus. This is because a pulse generator CPG produces a clock pulse (i.e., a third clock pulse) to be used in the bus cycle of the third internal bus by dividing the system clock for determining the bus cycles of the first and second internal buses, so that the signal of the third internal bus

can be transmitted as it is to the second internal bus. On the contrary, the bus state controller BSC synchronizes the signal on the second internal bus with the third clock pulse by delaying the signal on the second internal bus, if necessary, when it transmits the signal on the second internal bus to the third internal bus.

Detailed Description Text (18):
Moreover, such function modules, e.g., the central processing unit CPU, the cache memory or the dynamic memory access controller DMAC that their bus cycles will not exert direct influences upon the performance and the function of the single-chip microcomputer. On the other hand, such function modules, e.g., the free running timer FRT, the serial communication interface SCI or the watch-dog timer WDT that their bus cycles will not exert direct influences upon the data processing are connected with the third internal bus for the low-speed bus cycles. As a result, any high-speed type peripheral module need not be developed or designed according to the speed-up of the central processing unit CPU, but the circuit of the single-chip microcomputer can be efficiently specified. Moreover, the operation clock to be fed to the function module such as the free running timer FRT, the serial communication interface SCI or the watch-dog timer WDT can be lowered to reduce the power dissipation of the single-chip microcomputer.

Detailed Description Text (21):
For the power supply, an external terminal Vcc is a terminal to be fed with the power potential of the circuit, and an external terminal Vss is a terminal to be fed with the ground (potential) of the circuit. For controlling the operation modes: external terminals MD0 to MD2 are terminals to be fed with the clock select signal; external terminals MD3 and MD4 are terminals to be fed with a signal for specifying the bus size in a space CS0; and an external terminal MD5 is a terminal to be fed with a signal for specifying the later-described slave/master modes. For the address bus, external terminals A0 to A26 are external address terminals. For the data bus, external terminals D0 to D31 are external input/output data terminals.

Detailed Description Text (43):
FIG. 6 is a detailed block diagram showing one embodiment of the aforementioned break controller UBC. In this embodiment, the following functions are added to the break controller UBC. As in the foregoing embodiment of FIG. 1, the central processing unit CPU is isolated from the dynamic memory access controller DMAC and the external bus interface OBIF by the bus division. In case, therefore, a miss hit occurs in the access to the cache memory, the external memory has to be accessed to fetch the data.

Detailed Description Text (44):
In response to a control signal C1, a bus transceiver transmits the address signal of a first address bus AB1 to a second address bus AB2. Specifically, if a miss hit occurs in the cache memory, the address signal of the address bus AB1 can be transmitted to the address bus AB2 in response to the control signal C1 to access the external memory through the external bus interface OBIF. The data read out of the external memory at this time are transmitted to the central processing unit CPU through a data memory CDM of the cache.

Detailed Description Text (48):
FIG. 7 is a block diagram showing one embodiment of the aforementioned bus state controller BSC. This bus state controller BSC manages an address space and outputs a control signal, if necessary, through the external bus interface OBIF so that an optimum access can be made in eight spaces. As a result, the bus state controller BSC can be directly connected with the various memories such as the dynamic type RAM, the synchronous dynamic type RAM or the pseudo-static type RAM and the peripheral data processor LSI.

Detailed Description Text (53):
The bus state controller BSC is provided with an interface to be directly connected with the dynamic type RAM. This interface makes possible: the multiplex outputting of the row/column addresses; the burst transfer at the read time; the high-speed page mode for the continuous access; the RAS down mode to the discontinuous accesses to an identical row address; and the generation of a TP cycle for retaining the RAS precharge time. There is further provided an interface which can be directly

connected with the synchronous dynamic type RAM. This interface makes possible: the multiplex outputting of the row/column addresses; the memory accesses by the burst read and single write; and the continuous column accesses by the bank active mode.

Detailed Description Text (57):
FIG. 8 is a block diagram for explaining an example of connection between the bus state controller BSC and the synchronous dynamic type RAM (as will be shortly referred to as the "SDRAM") by the external bus interface OBIF. In FIG. 8, there is also shown an example of connection of the static type RAM (as will be shortly referred to as the "SRAM") as a basic memory.

Detailed Description Text (63):
FIG. 12 is a block diagram for explaining the connection between the bus state controller BSC and the dynamic type RAM (which will be shortly referred to as the "DRAM") by the external bus interface OBIF. The DRAM, as shown, has a construction of .times.16 bits and can be accessed by the high order byte and the low order byte according to the two-CAS method (/UCAS* /LCAS).

Detailed Description Text (65):
FIG. 14 is a block diagram for explaining an example of connection between the bus state controller BSC and the pseudo-static type RAM (as will be shortly referred to as the "PSRAM") by the external bus interface OBIF. The output/RAS*/CE at the single-chip microcomputer MCU is connected with the chip enable terminal /CE of the PSRAM, and the output /CAS*/OE at the side of the MPU is connected with the output enable*refresh control terminal /OE*/RFSH of the PSRAM. The write enable terminal /WE of the PSRAM is connected as in the SRAM with the terminal /WEj of the MCU. Moreover, the chip select terminal /CS of the SRAM is fed with the terminal /CSn of the MCU. Specifically, the PSRAM is assigned by the aforementioned space division to the space CS3, and the SRAM at this time is assigned to the remaining spaces.

Detailed Description Text (68):
Specifically, in an ordinary microcomputer system, the main bus is constructed of a memory control unit for accessing a high-speed memory such as a main memory or an extension memory, a DRAM or SDRAM as the main memory, a ROM stored with a basic control program, and a keyboard controller connected at its leading end with a keyboard. Moreover, the main bus is connected with a display adapter, which in turn is connected at its leading end with a display unit such as the CRT or LCD. The main bus is further connected with a parallel port, a serial port such as mouse, a floppy disc drive, and a buffer controller for conversion into a hard disc interface through the main bus. On the other hand, the bus from the aforementioned memory control unit is connected with an extended RAM and a main memory. FIG. 15 is so simplified that only the SDRAM is shown as the main memory.

Detailed Description Text (73):
FIG. 16 is a timing chart showing the case in which the SDRAM on the main bus is to be accessed from the S-MCU. When the signal /BREQ is outputted from the slave side whereas the bus use acknowledge signal /BGR is outputted from the main side to set the signal /BACK to the low level, a row address (ROW) and a column address (COLUMN) are outputted as in case the aforementioned SDRAM is accessed. At the master side, the address and the command are transmitted with a delay (of one clock) through the latched bus buffers BB1 and BB2 so that the read data is also transmitted with a delay through the latched bus buffer BB2 to the slave side.

Detailed Description Text (75):
The cache memory has its circuit constructed roughly of a cache tag (i.e., address array), a cache data (i.e., data array) and a cache controller. The cache tag stores a portion of the address called the "address tag", and the cache data stores the data corresponding to the address tag stored in the cache tag. As a result, when a portion of the address stored in the cache tag matches the corresponding address coming from the central processing unit CPU, the hit signal is outputted from the cache tag so that the data read out of the cache data being selected in parallel is fetched by the central prodessing unit CPU. If a miss hit occurs, an external main memory is accessed through the aforementioned break controller UBC and external bus interface.

Detailed Description Text (104):
FIG. 22 is a schematic block diagram showing one embodiment of the DMAC and its peripheral portion according to the present invention. The DMAC according to the present invention is connected with the internal bus B2 (AB2, DB2) of the single-chip microcomputer according to the present invention. The DMAC executes the data transfers between the external memories (ROM, RAM) or the external input/output devices, which are connected with the external bus B4 (AB4, DB4) through the aforementioned external bus interface OBIF, and the internal peripheral modules which are connected with the cache memory or the internal bus B3 (AB3, DB3), although shown not in FIG. 22 but in FIG. 1.

Detailed Description Text (113):
The aforementioned divider unit DIVU performs divisions over about 38 cycles, for example, while being isolated from the internal bus B2 (AB2, DB2) by the bus interface, as shown in FIG. 1. Thus, the central processing unit CPU or the like can perform the data processing or the like using the internal bus B2 (AB2, DB2) in parallel.

Detailed Description Text (135):
If, therefore, the single-chip microcomputer is equipped with an external data bus having a size of 64 bits, the data bus can be directly connected to the main memory of two-bank construction so that no data buffer is required. On the other hand, the pin number increases to raise the package cost. Moreover, the chip area may be increased by the limit to the gap between the bonding pads. For this reason, it is troublesome to shorten the average access time by using the DRAM of the high-speed page mode. If the SRAM is used, the continuous accesses for each cycle can be accomplished but fail to match the cost. In order to shorten the average access time at a low cost, it is most appropriate to adopt the internal cache memory, as in the foregoing embodiment.

Detailed Description Text (175):
The address bus and the data bus in the chip are wired in most of the modules. These buses have an electrostatic capacity is of an order of several pF. If individual thirty two address buses and data buses are driven to the opposite polarity for each cycle, the current to be consumed by the charge/discharge exceeds 60 mA, and the delay increases as the electrostatic capacity rises.

Detailed Description Text (177):
FIG. 33 is a timing chart for explaining the individual bus cycles in the single-chip microcomputer according to the present invention. The individual signals of the cache buses AB1 and DB1 (i.e., the aforementioned first internal bus of FIG. 1) and the internal buses AB2 and DB2 (i.e., the aforementioned second internal bus of FIG. 1) will change in synchronism with the high-level period of the clock, whereas the individual signals of the external buses AB4 and DB4 (i.e., the aforementioned fourth bus of FIG. 1) connected with the outside of the chip will change in synchronism with the low-level period of the clock.

Detailed Description Text (178):
In case the CPU accesses the data or instruction on the memory, it outputs an address signal to the cache address bus AB1 in synchronism with a clock signal (Clock) and raises the (not-shown) access signal for indicating execution of the address to the high level. In response to this, the cache memory retrieves internal cache memories. In the next cycle, the cache memory outputs the data read out of the cache data memory to the cache data bus DB1 in synchronism with the clock signal and raises the ready signal to the high level to inform the CPU of the end of the data access. This is indicated in FIG. 33 by the access at an address A and the access at an address (A+4).

Detailed Description Text (180):
The external bus interface (as designated at OBIF in FIG. 1) decodes the value of the internal address bus (AB2) in response to the high level of the aforementioned access signal and decides whether it is an access to the inside or outside of the chip. Since the address signal C has an address outside of the chip, it is instantly superposed on the external address bus (AB4) to raise the external bus access signal to the high level.

Detailed Description Text (181):
Since the preparation for reading the data is not ended in the next cycle, the internal ready signal is set to the low level to inform the cache memory of the fact that the data is not prepared. The external bus interface OBIF outputs the read data to the internal data bus (AB2, DB2) at the cycle 6, in which the read is ended, and raises the internal ready signal to the high level to inform the cache memory of the read end. The cache memory writes the data of the internal bus (AB2, DB2) therein and outputs it to the cache data bus (DB1). At the same time, the cache memory raises the cache ready signal to the high level to inform the CPU of the read end. During the time period (i.e., the cycles 5 and 6) in which the cache ready signal is at the low level, the CPU interrupts updating of the address bus AB1.

Detailed Description Text (183):
In case the CPU is going to access the peripheral modules to be connected with the peripheral bus (e.g., the third internal bus of FIG. 1) such as the free running timer FRT, the serial communication interface SCI and the watch-dog timer WDT, the address signal B to be outputted from the cache address bus AB1 through the cache memory to the internal address bus AB2 acts as the address signal B for those peripheral modules. This address signal B is outputted through the bus state controller BSC to the peripheral address bus AB3. Simultaneously with this, the bus access signal is raised to the high level.

Detailed Description Text (184):
After the data output of the peripheral data bus DB3 from the peripheral modules or the write end of the data of the peripheral data bus DB3 in the peripheral modules, the external bus interface OBIF raises the internal bus ready signal to the high level to inform the end of the access. Simultaneously with this, in the data reading case, the read data on the peripheral data bus DB3 is outputted from the bus state controller BSC to the internal data bus DB2.

Detailed Description Text (187):
When the signals of those four control lines are at the low level, the synchronous DRAM fetches the value of the address bus AB4 in synchronism with the rising edge of the clock and writes it as it is in the internal mode setting register. As a result, a desired mode setting can be easily accomplished by accessing a suitable one of the aforementioned addresses FFFF8000 to FFFB000. The control signal at the aforementioned timing is produced by the aforementioned memory control signal generator MCTG shown in FIG. 7. Specifically, this production can be realized by providing the area control unit or the like of the bus state controller BSC with a suitable address decoder and by establishing a sequence state for lowering the signals of the aforementioned four memory control lines to the low level under the aforementioned address decoding conditions.

Detailed Description Text (252):
Moreover, there are juxtaposed the timets FRT and WDT and the serial communication interface SCI which are connected with the not-shown third bus (AB3, DB3). These peripheral modules can have their occupied areas reduced by using those existing circuits as they are, which have their output circuit operations relatively delayed by delaying their bus cycles. In the periphery of the chip, there are arranged: a region P for forming bonding pads to be coupled to the aforementioned external terminals (as shown in FIGS. 2 and 3); and a region B for forming the input buffer, the output buffer and the input/output buffer corresponding to the bonding pads.

Detailed Description Text (259):
(1) The internal bus is divided into three: the first bus is connected with the central processing unit and the cache memory, and the second bus is connected with the dynamic memory access controller and the external bus interface. The first bus and the second bus are equipped with the break controller having a bus transceiver function to connect the first address bus and the second address bus selectively. The third bus is connected with peripheral modules and given a lower speed than the first and second bus cycles. There is provided the bus state controller for data transfers and synchronizations between the second bus and the third bus. As a resultant effect, the load capacity of a signal transmission path can be reduced to effect the signal transmissions at a high speed. Moreover, the consumption of

current through the peripheral modules required to have no high operation speed can be reduced because the peripheral modules are isolated.

Detailed Description Text (264):
(6) The aforementioned external bus interface is given the burst read mode and the single-write mode of the synchronous dynamic type RAM, and the interface function to access the dynamic type RAM and the pseudo-static type RAM directly. As a resultant effect, the synchronous dynamic type RAM, the dynamic RAM and the pseudo-static type RAM can be directly connected by the external bus interface, to improve the user-friendliness.

Detailed Description Text (265):
(7) The clock pulse is produced with a phase delay from the clock pulse of the external bus interface and is fed to the central processing unit. As a resultant effect, the setup/hold time of the synchronous dynamic type RAM can be retained to extend the operation margin.

Detailed Description Text (267):
(9) The external bus interface is equipped with the memory control signal generator for generating the control signal necessary for setting the operation mode of the synchronous dynamic type RAM by using an address signal partially, when the central processing unit is started by accessing the predetermined access space to set the row address strobe signal, the column address strobe signal and-the write enable signal to the low level. As a resultant effect, the synchronous dynamic type RAM can have its modes easily set by the central processing unit.

Detailed Description Text (275):
(17) The aforementioned three-dimensional image processing is carried out by the single-chip microcomputer which comprises: the central processing unit and the multiply and accumulate arithmetic unit connected with the first bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external bus interface; the break controller connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the address bus of the second bus; the peripheral modules connected with the third bus having a lower-speed bus cycle than the first and second bus cycles; and the bus state controller for effecting the signal transfers and the synchronization between the second bus and the third bus. As a resultant effect, a high-speed three-dimensional image processing can be realized by the relatively simple construction.

Detailed Description Text (282):
Specifically, the internal bus is divided into three: the first bus is connected with the central processing unit and the cache memory, and the second bus is connected with the dynamic memory access controller and the external bus interface. The first bus and the second bus are equipped with the break controller having a bus transceiver function to connect the first address bus and the second address bus selectively. The third bus is connected with peripheral modules and given a lower-speed bus cycle than the first and second bus cycles. There is provided the bus state controller for data transfers and synchronizations between the second bus and the third bus. As a result, the load capacity of a signal transmission path can be reduced to effect the signal transmissions at a high speed. Moreover, the consumption of current through the peripheral modules required to have no high operation speed can be reduced because the peripheral modules are isolated.

Detailed Description Text (286):
The aforementioned external bus interface is given the burst read mode and the single-write mode of the synchronous dynamic type RAM, and the interface function to access the dynamic type RAM and the pseudo-static type RAM directly. As a result, the synchronous dynamic type RAM, the dynamic RAM and the pseudo-static type RAM can be directly connected by the external bus interface, to improve the user-friendliness.

Detailed Description Text (287):
The clock pulse is produced with a phase delay from the clock pulse of the external bus interface and is fed to the central processing unit. As a result, the setup/hold

time of the synchronous dynamic type RAM can be retained to extend the operation margin.

Detailed Description Text (289):
The external bus interface is equipped with the memory control signal generator for generating the control signal necessary for setting the operation mode of the synchronous dynamic type RAM by using an address signal partially, when the central processing unit is started by accessing the predetermined access space to set the row address strobe signal, the column address strobe signal and the write enable signal to the low level. As a result, the synchronous dynamic type RAM can have its modes easily set by the central processing unit.

Detailed Description Text (297):
The aforementioned three-dimensional image processing is carried out by the single-chip microcomputer which comprises: the central processing unit and the multiply and accumulate arithmetic unit connected with the first bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external bus interface; the break controller connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the address bus of the second bus; the peripheral modules connected with the third bus having a lower-speed bus cycle than the first and second bus cycles; and the bus state controller for effecting the signal transfers and the synchronization between the second bus and the third bus. As a result, a high-speed three-dimensional image processing can be realized by the relatively simple construction.